



T.C.SANJEEVARAYUDU M.Tech.

Assistant Professor of ECE (Adhoc),

JNTUA College of Engineering(Autonomous)

Pulivendula – 516390, Andhra Pradesh, India

Bio-data

Name : **T.C.SANJEEVARAYUDU**

Official Address : **Assistant Professor of ECE ,
Jawaharlal Nehru Technological University Anantapur
Pulivendula – 516390, Andhra Pradesh (India) Mobile
: 091-9493249046**

Residential Address : **D.No:10/119 A,
Peddapasupula,
peddamudium,ysr kadapa
– 516411

Andhra Pradesh (India)**

E-mail : **tappetasanjeev@gmail.com**

Nationality : Indian

Religion : Hindu

Educational Qualifications:

S. No.	Qualification	University/Institution	Specialization	Year of award
1.	M.Tech	JNTU Anantapur	VLSI System Design	2011
2.	B.Tech	JNTU Anantapur	ECE	2009

Teaching Experience: 11+ years of teaching UG & PG Courses

Subjects Taught:

Undergraduate courses	Post graduate courses
-----------------------	-----------------------

<ul style="list-style-type: none"> ❖ Electronic Devices and Circuits ❖ Electronic Circuit Analysis ❖ Pulse & Digital Circuits ❖ Digital Logic and Design ❖ Digital Signal Processing ❖ Analog Electronic Circuits ❖ Microprocessors and Microcontrollers ❖ Basic Electrical and Electronics Engineering ❖ Optical Fiber Communications ❖ Electronic Measurements and Instrumentation ❖ Advanced 3G& 4G Wireless Mobile communications ❖ Embedded systems ❖ Radar and Navigational Aids 	<ul style="list-style-type: none"> ❖ Digital Communication Techniques ❖ Detection and Estimation Theory ❖ Mobile Networks ❖ Adaptive Signal Processing
---	--

- ❖ In addition, the laboratories of UG and PG programmes in the areas of Electronics and Computers have been dealt with.

Number of Research publications:

International Journals	:	04
International Conferences	:	03

List of publications:

International Journals:

- The paper titled “**An Efficient and Improved Radix-16 Based Booth Multiplier for 64-Bit Based on the Reduced Height of Partial Product Array**” International Journal of Emerging Technologies and Innovative Research (JETIR) ON 04 April 2019.
- The paper titled “**Shift Register With Low Power And Area Efficient Pulsed Latches** ” International Journal ON May 23rd 2023.
- The paper titled “**A Novel Approach For Breast Tumor Detection And Segmentation From MRI Images Using Image Processing Techniques**” International Journal ON August 2023.

- The paper titled “**A Novel Approach For Breast Tumor Detection And Segmentation From MRI Images Using Image Processing Techniques**” International Journal ON August 2023.

International Conferences

- ❖ The paper titled “**Fibonacci Numeral System (FNS) Based on Chip Cross Talk Avoidance High Speed Open System**” International conference on explorations an innovations in engineering & technology (ICEIET -2016) ON 18th & 19th March 2016.
- ❖ The paper titled “**Design and implementation of single stage fully differential class AB Amplifier with Adaptive Biasing**” National conference on explorations an innovations in engineering & technology (ICEIET -2016) ON May 2018.
- ❖ The paper titled “**Design of Dual band L-SLOT Microstrip patch Antenna for Wireless Communications**” International conference on explorations an innovations in engineering & technology (ICEIET -2016) 28th-29th February 2020.

Workshops attended:

- ❖ Participated in one day FDP on “**SCADA**” conducted 16th March 2023.
- ❖ Participated in one day FDP on “**Design Of Electrical vehicalls By Using MATLAB**” conducted 17th March 2023.
- ❖ Participated in five day FDP on “**Design And Implementation Of Adavanced VLSI Architectures**” conducted conducted 13th March 2023 to 17th March 2023.
- ❖ Participated in five day FDP on “**Congnitive Computing**” conducted 20th March 2023 to 23rd March 2023.
- ❖ Participated in three day FDP on “**Engineering Graphics Through Auto CAD software**” conducted 21st April 2023 to 23rd April 2023.
- ❖ Participated in one month FDP on “**WEB DEVELOPMENT USING REACT JS**” conducted from 4th jan 2023 to 03rd jan 2023.
- ❖ Participated in one month FDP on “**Pythhon FullStack Development**” conducted from 28th Feb 2023 to 29th March 2023.
- ❖ Participated in one month FDP on “**Embedded Systems**” conducted 27th March 2023 to 27th April 2023.
- ❖ Participated in one week online FDP on “**Machine Learning Algorithem For Dead Time Systems (MLADTS)**” conducted 24th jan 2022 to 29th jan 2022.
- ❖ Participated in one week online FDP on “**Research Methodology Design and Innovation**” conducted 16th dec 2022 to 21st dec 2022.
- ❖ Participated in one month FDP on “**Artificial Intelligence 3.0 Master class**” conducted 23rd nov 2022 to 22nd dec 2023 .
- ❖ Participated in one week online FDP on “**Ecad For Buildinds**” conducted 10th october to 16th october2022.
- ❖ Participated in two day FDP on “**Introduction to web development**” conducted 17th july 2020 to 19th july 2020.

- ❖ Participated in one day FDP on “**Research Paper writing & citation manager**” conducted 21st June 2020.
- ❖ Participated in two weeks FDP on “**Matlab Tools & their applications in Engineering**” conducted 25th May 2020 to 7th June 2020.
- ❖ Participated in five day FDP on “**Recent Communications Tools & its Application**” conducted 19th May 2020 23rd May 2020.
- ❖ Participated in two day FDP on “**Introduction to web development**” conducted 17th July 2020 to 19th July 2020.
- ❖ Participated in two day FDP on “**Research Methodology in Science and Technology**” conducted from 17th -18th October 2016 at JNTUACEP, Pulivendula.
- ❖ Participated in two day FDP on “**Digital Image Processing, Pattern Recognition and its Applications**” conducted from 19th -20th September 2016 at JNTUACEP, Pulivendula .
- ❖ Participated in five day FDP on “**VLSI Design Flow Using Xilinx Vivado Targeting Xilinx 7-series FPGA and Zynq SoC Architecture**” conducted from 6th -10th September 2016.
- ❖ Participated in two day FDP on “ **VLSI Design Advancements using Xilinx Tools**” conducted from 26th -27th August 2016 at JNTUACEP, Pulivendula.
- ❖ Participated in two day FDP on “**Internet of Things-Hands on Training**” conducted from 14th– 15th March 2016.JNTUACEP, Pulivendula
- ❖ Participated in two day FDP on “**Linear integrated circuits: A system Approach**” conducted from 25th -26th September 2015 at JNTUACEP by Texas.
- ❖ Participated in five day FDP on “**Advanced digital signal processing** “conducted from 27th -31st July 2015 at NIT, Warangal.
- ❖ Participated in one day FDP on “**Human values and ethics**” conducted on 1st July 2015 at JNTUACE, Ananthapuramu

Declaration:

I hereby declare that the information furnished above is true to the best of knowledge

(T.C.Sanjeeva Rayudu)

Date: -07-2022

Pulivendula.