JNTUA COLLEGE OF ENGINEERING (AUTONOMUS): PULIVENDULA
Department of Computer Science & Engineering
B.Tech II Year I Semester

Subject: Computer Organization

Lesson plan

Course Code	**:**	15ACS07			
Course Title	**:**	**Computer Organization**			
Course Structure	**:**	Lectures	Tutorials	Practicals	Credits
		4	0	-	3
Course Coordinator	**:**	Sri M. Chenna Keshava, Assistant Professor (Adhoc)			
Team of Instructor		Dr. G. Murali			

I. Course Overview

This course deals with computer Organization and Design. Computer organization is concerned with the structure way the hardware components are connected together to form a computer system. Computer design is concerned with development of the hardware for the computer taking into consideration a given set of specifications. This course helps the students to get the knowledge on basic understanding of Computer organization, design, and programming of a simple digital computer. And also this course provides the organization and architecture of the separate functional units of the digital computer.

II. Prerequisite(s):

Level	Credits	Periods / Week	Prerequisites
UG	3	4	Basics(Hardware) of a computer

III. Assessment:

FORMATIVE ASSESMENT	
Mid Semester Test I (Theory) for 20 Marks in first two units is conducted at the end of 9th week. Mid Semester Test II (Theory) for 20 Marks in last three units is conducted at the end of the course work.	20 Marks
Multiple Choice Test I for 10 Marks in first two and halfunits is conducted at along with Theory exam. Multiple Choice Test II for 10 Marks in last two and	10 Marks

halfunits is conducted at along with Theory exam. Note: After evaluating these tests 30 marks are calculated as 80% from best marks and 20% from other.	
Total (Formative)	30 Marks
SUMMATIVE ASSESMENT	
End Semester Examination in all units is conducted for 70 Marks	70 marks
Grand Total	100 Marks

IV. Course objectives:

I. To gain methodical understanding of the basic structure and operation of a digital computer.

II. To learn the fundamentals of computer organization and its relevance to classical and modern problems of computer design.

III. To make the students understand the structure and behavior of various functional modules of a computer.

IV. To explore the hardware requirements for cache memory and virtual memory for better understanding of memory management.

V. To understand the techniques and that computers use to communicate with I/O devices.

VI. To study the concepts of pipelining and the way it can speed up processing.

VII. To understand the basic characteristics of multiprocessors.

V. Course Outcomes:

1. Optimize the algorithms to exploit pipelining and multiprocessors.
2. Algorithm design for bit level arithmetic.
3. Ability to use memory and I/O devices effectively.

VI. Program outcomes:

a An ability to apply knowledge of computing, mathematical foundations, algorithmic principles, and computer science and engineering theory in the modeling and design of computer-based systems to real-world problems (fundamental engineering analysis skills)

b An ability to design and conduct experiments, as well as to analyze and interpret data (information retrieval skills)

c An ability to design , implement, and evaluate a computer-based system, process, component, or program to meet desired needs, within realistic constraints such as economic, environmental, social, political, health and safety, manufacturability, and sustainability (Creative Skills)

d An ability to function effectively on multi-disciplinary teams (team work)

e An ability to analyze a problem, identify, formulate and use the appropriate computing and engineering requirements for obtaining its solution (engineering problem solving skills)

f An understanding of professional, ethical, legal, security and social issues and responsibilities (professional integrity)

g An ability to communicate effectively both in writing and orally (speaking / writing skills)

h The broad education necessary to analyze the local and global impact of computing and engineering solutions on individuals, organizations, and society (engineering impact assessment skills)

i Recognition of the need for, and an ability to engage in continuing professional development and life-long learning (continuing education awareness)

j A Knowledge of contemporary issues (social awareness)

k An ability to use current techniques, skills, and tools necessary for computing and engineering practice (practical engineering analysis skills)

l An ability to apply design and development principles in the construction of software and hardware systems of varying complexity (software hardware interface)

m An ability to recognize the importance of professional development by pursuing postgraduate studies or face competitive examinations that offer challenging and rewarding careers in computing (successful career and immediate employment).

VII. Syllabus:

UNIT - I : Introduction to Computer Organization and Architecture Basic Computer Organization – CPU Organization – Memory Subsystem Organization and Interfacing – I/O Subsystem Organization and Interfacing – A Simple Computer Levels of Programming Languages, Assembly Language Instructions, Instruction Set Architecture Design, A simple Instruction Set Architecture

UNIT – II: Central Processing Unit: Introduction, General Register Organization, Stack Organization, Instruction formats –Addressing Modes – Data Transfer and Manipulation – Program Control. **Computer Arithmetic:** Addition and Subtraction – Multiplication Algorithms – Division Algorithms –Floating-Point Arithmetic Operations – Decimal Arithmetic unit

UNIT – III: Register Transfer: Register Transfer Language – Register Transfer – Bus and Memory Transfers –Arithmetic Micro operations – Logic Micro operations – Shift Micro operations. **Control Unit:** Control Memory – Address Sequencing – Micro program Example – Design of Control Unit

UNIT – IV: Memory Organization: Memory Hierarchy – Main Memory – Auxiliary Memory – Associative Memory – Cache Memory – Virtual Memory. **Input/output Organization:** Input-Output Interface – Asynchronous Data Transfer – Modes of Transfer – Priority Interrupt – Direct Memory Access (DMA).

UNIT – V: Pipeline: Parallel Processing – Pipelining – Arithmetic Pipeline – Instruction Pipeline. **Multiprocessors:** Characteristics of Multiprocessors – Interconnection Structures – Inter Processor Arbitration – Inter Processor Communication and Synchronization

Text Books:

1. “Computer Systems Organization and Architecture”, John D. Carpinelli, PEA, 2009.

2. “Computer Systems Architecture”, 3/e, M. Moris Mano, PEA, 2007

Reference Books:

1. “Computer Organization”, Carl Hamacher, ZvonksVranesic, SafeaZaky, 5/e, MCG, 2002.
2. “Computer Organization and Architecture”, 8/e, William Stallings, PEA, 2010.
3. “Computer Systems Architecture a Networking Approach”, 2/e, Rob Williams.
4. “Computer Organization and Architecture” Ghoshal, Pearson Education, 2011.
5. “Computer Organization and Architecture”, V. Rajaraman, T. Radakrishnan.

6. “Computer Organization and Design”, P. Pal Chaudhuri, PHI
7. “Structured Computer Organization”, Andrew S. Janenbaum, Todd Austin

IX. Course Plan:

The course plan is meant as a guideline. There may probably be changes.

Lecture No.	Course Learning Outcomes	Topics to be covered	Reference
1, 2	Understanding the structure and operations of components in Computer and CPU.	**UNIT – I** **Introduction to Computer Organization and Architecture** Basic Computer Organization, CPU Organization	T1:4.1, T1:4.2
3, 4	The student gain the knowledge on components of memory system and how the system provides the interface.	Memory Subsystem Organization and Interfacing	T1:4.3
5, 6	The structure of organization and how the I/O system provides interface and also student have the ability to trouble shoot the problems, occurred in these components.	I/O Subsystem Organization and Interfacing	T1:4.4
7, 8	Programming ability on Assembly language and basic Languages.	A Simple ComputerLevels of Programming Languages,Assembly Language Instructions,	T1:3.1,T1:3.2,3.4, R1:2.6
9,10	Ability to design the Structure of Instructions, which are executed by the system.	Instruction Set Architecture Design, A simple Instruction Set Architecture	T1:3.3,3.4, R2:10.2, R5:8.13
11,12	Will understand the stages of an instruction and how it executes. And also gain the knowledge of various types of memory reference instructions. And also summarizes the flowchart of all the micro instructions.	**UNIT – II** **CPU Design:** Instruction Cycle. Memory-Reference Instructions.	T2:5.5,5.6
13	Will understand how the communication in between input and output components of the computer through the interrupt	Input/output and Interrupt	T2:5.7
14	Student will understand the various addressing modes and based on modes the operands are accessed.	Addressing Modes	T2:8.5, W2.1, R1:2.5, R5:7.4

15,16	Gain the knowledge of,how the data transfer is and computational capabilities of the computer.	Data Transfer and Manipulation, Program Control.	T2:8.6 T2:8.7
17,18	Able to implement the algorithms for computer	**Computer Arithmetic:** Addition and Subtraction	T2:10.2, R5: 4.5, 4.6,
19,20	Gain the knowledge of multiplication and division algorithms and also how to implement the algorithms.	Multiplication Algorithms, Division Algorithms	T2:10.3,10.4, R1:6.4, 6.5, 6.6, R5:4.7, 4.9
21,22	Gain the knowledge on structure of floating point arithmetic operations and implementation of operations for the system. And also know the arithmetic operations of decimal system.	Floating-Point Arithmetic Operations, Decimal Arithmetic unit	T2: 10.5,10.6, R1:6.7.1, R5:4.11,4.12,4.13
23,24	Will be able to know the various hardware logic circuits and notations to represent the operations performed on the circuits.	**UNIT – III** **Register Transfer:** Register Transfer Language, Register Transfer	T2:4.1, T2:4.2, R1:7.1.1,
25,26	Will understand the transfer mechanism in between memory components through various buses.	Bus and Memory Transfers	T2:4.3, R1:7.3
27,28	Student will understand the structure of circuits to perform the micro operations by a computer.	Arithmetic Micro operations.	T2:4.4
29,30	Ability to design the circuits for different various micro operations.	Logic Micro operations, Shift Micro operations.	T2:4.5,4.6
31,32	Student will understand the computer is controlled either by hardwired or micro programmed control system.	**Control Unit:** Control Memory	T2:7.1, R1:7.4, R6:5.4
33,34	Gain the knowledge of execution process of control instructions	Address Sequencing	T2:7.2
35,36	Ability to implement a control unit to control the system.	Micro program Example, Design of Control Unit	T2:7.3,7.4, R1:7.5, R6:5.5
37,38	Student get the clear about the various memory components and their capabilities, sizes, operations	**UNIT – IV** **MemoryOrganization:** Memory Hierarchy, Main Memory.	T2:12.1,12.2, R1:5.2, 5.3, 5.4, R6:5.3
39,40	Student gain the knowledge on structure and design and work nature of various memory components	Auxiliary Memory, Associative Memory	T2:12.3,12.4, R1:5.9, R6: 6.7,7
41,42		Cache Memory, Virtual Memory.	T2:12.5,12.6, w4.1, w4.2, R1: 5.5, 5.6, 5.7, R3:18.4,

			R5:10.5,10.6,10.7, 10.8, R6:5.5,6.8
43,44	Understanding the communication and structure in between input and output components.	**Input/output Organization:** Input-Output Interface.	T2:11.2, R1:10.1,10.2, R5:11, R6:8
45,46	Gain the knowledge on various methods to transfer the data.	Asynchronous Data Transfer, Modes of Transfer	T2:11.3,11.4,R1:10.3
47,48	Understanding the accessing nature in Direct Memory Access.	Priority Interrupt, Direct Memory Access (DMA).	T2:11.5,11.6, R1:4.4
49,50	Have the ability to process a procedure with better execution time.	**UNIT – V** **Pipeline:** Parallel Processing, Pipelining.	T2:9.1,9.2, R1:12.1,8.1.2, R5:12.5, R3:2.23, R6:10.6
51,52	Understanding the stages in arithmetic and instruction pipeline.	Arithmetic Pipeline, Instruction Pipeline.	T2:9.3,9.4, R`1:8.2,8.3,8.4
53,54, 55	Having the ability to combine multiple processors by knowing the various internal organizations.	**Multiprocessors:** Characteristics of Multiprocessors, Interconnection Structures	T2:13.1,13.2, R1:12.2, 12.4, 12.7, R5:13.4
56,57	Gain the knowledge on work of the inter processor.	Inter Processor Arbitration	T2:13.3
58,59,60	Having the ability to control the communication in processing.	Inter Processor Communication and Synchronization	T2:13.4

X. Mapping course outcomes leading to the achievement of the programme outcomes:

Course Outcomes	**Program Outcomes**											
	a	**b**	**C**	**d**	**e**	**f**	**g**	**h**	**i**	**j**	**k**	**l**
1	**H**		**S**									
2		**H**			**S**							
3					**S**	**H**						

S= Supportive
H=Highly Related

Justification of Course syllabus covering Course Outcomes:

By covering the syllabus a student can understand the designing of algorithm and flowcharts. Student is able to develop applications using C Program Constructs.

Justification of CO's –PO's Mapping Table:

By mapping CO-1 to the PO's E which are related to the course CO1: The student is able to analyze and Implement Problems

By mapping CO-2 to the PO's A, which are related to the course CO2: The student is able to design algorithm and draw the flowcharts for different types of problems

By mapping CO-3 to the PO's C & M which are related to the course CO3: The student is able to understand the purpose of different programming Constructs.

By mapping CO-4 to the PO's E which are related to the course CO4: The student is able to understand the Purpose of arrays and Applications of arrays?

By mapping CO-5 to the PO's K & M which are related to the course CO5: The student is able to understand the Purpose of Functions, advantages and their applications

By mapping CO-6 to the PO's E which are related to the course CO6: The student is able to understand the concept of structures, Applications and advantages.

By mapping CO-7 to the PO's E which are related to the course CO7: The student is able to differentiate iteration and Recursion.

By mapping CO-8 to the PO's C which are related to the course CO8: The student is able to understand Scope and Life time of the variables

By mapping CO-9 to the PO's K which are related to the course CO9: The student is able to understand the purpose of Secondary storage and advantages; He is able to write programs using file Constructs.

By mapping CO-10 to the PO's I & M which are related to the course CO10: The student is able to develop applications using C programming constructs and this knowledge will help him in further studies and industry needs.

Faculty Sign **HOD**